CLAIMS

1. A method for performing path extraction within a design analysis tool, comprising:

providing a first set of paths corresponding to a circuit design, the first set of paths having single-path components and multiple-path components; and

extracting a second set of paths from the first set of paths, the second set of paths having no multiple-path components.

2. The method of claim 1, wherein the first set of paths extends from a launch point of the circuit design to a capture point of the circuit design.

3. The method of claim 2, wherein the launch point comprises a first latch and the capture point comprises a second latch.

4. The method of claim 1, wherein the single-path components and multiple-path components comprise combinational logic elements.

5. The method of claim 1, wherein the multiple-path components include single-path components.

6. The method of claim 1, wherein each of the multiple-path components comprises a plurality of component paths, and the second set of paths is extracted from the plurality of component paths.

7. The method of claim 6, wherein extracting the second set of paths comprises combining a first component path from one of the multiple-path components with a second component path from another one of the multiple-path components.

8. A method for identifying false paths, comprising:
providing a path corresponding to a circuit design;
determining whether a set of final value conditions are satisfied;
determining whether a set of side value propagation conditions are satisfied;
determining whether a set of initial value conditions are satisfied;
determining whether the path is false based on at least one of the set of final value conditions, the set of side value propagation conditions, and the set of initial value conditions.

9. The method of claim 8, further comprising:
determining whether a set of slower path conditions are satisfied, and wherein determining whether the path is false is based on

at least one of the set of final value conditions, the set of side value propagation conditions, and the set of initial value conditions, and the set of slower path conditions.

10. The method of claim 8, wherein the set of final value conditions and the set of side value propagation conditions correspond to a first time frame and the set of initial value conditions corresponds to a second time frame, different from the first time frame.

11. The method of claim 8, further comprising:

providing a first set of paths corresponding to the circuit design, the first set of paths having single-path components and multiple-path components; and

extracting a second set of paths from the first set of paths, the second set of paths having no multiple-path components; and

selecting the path from the second set of paths.

12. The method of claim 8, wherein at least one of determining whether a set of final value conditions are satisfied, determining whether a set of side value propagation conditions are satisfied, and determining whether a set of initial value conditions are satisfied, is performed by an automatic test pattern generation (ATPG) tool.

13. A method for false path identification within a circuit design, comprising:

receiving a first set of paths corresponding to the circuit design;

providing a set of conditions corresponding to at least one path of the first set of paths to an automatic test pattern generation (ATPG) tool, the ATPG tool having an ATPG model corresponding to at least a portion of the circuit design;

the ATPG tool generating a response to the set of conditions using the ATPG model; and

identifying a false path within the first set of paths based on the response from the ATPG tool.

14. The method of claim 13, further comprising after receiving the first set of paths, translating the first set of paths.

15. The method of claim 13, further comprising:

after receiving the first set of paths, extracting a second set of paths from the first set of paths, wherein the set of conditions corresponds to at least one path of the second set of paths.

16. The method of claim 13, wherein the set of conditions comprises at least one of final value conditions, initial value conditions, side propagation value conditions, and slower path conditions.

17. The method of claim 16, wherein the response to the set of conditions from the ATPG tool indicates whether the set of conditions is satisfied.

18. The method of claim 13, wherein the false path is fed back to the static analysis tool.

19. The method of claim 13, wherein the ATPG tool is a commercially available ATPG tool.

20. The method of claim 13, wherein receiving the first set of paths comprises receiving the first set of paths from a static analysis tool.

21. A design analysis tool capable of identifying false paths, stored via a computer readable medium, said computer readable medium comprising:

a first plurality of instructions for receiving a path corresponding to a circuit design;

a second plurality of instructions for determining whether a set of final value conditions are satisfied;

a third plurality of instructions for determining whether a set of side value propagation conditions are satisfied;

a fourth plurality of instructions for determining whether a set of initial value conditions are satisfied; and

a fifth plurality of instructions for determining whether the path is false based on at least one of the set of final value conditions, the set of side value propagation conditions, and the set of initial value conditions.

22. The computer readable medium of claim 21, further comprising:

a sixth plurality of instructions for determining whether a set of slower path conditions are satisfied, and wherein the fifth plurality of instructions comprises instructions for determining whether the path is false is based on at least one of the set of final value conditions, the set of side value propagation conditions, and the set of initial value conditions, and the set of slower path conditions.

23. The computer readable medium of claim 21, further comprising:

a sixth plurality of instructions for providing a first set of paths corresponding to the circuit design, the first set of paths having single-path components and multiple-path components; and

a seventh plurality of instructions for extracting a second set of paths from the first set of paths, the second set of paths having no multiple-path components; and

a eighth plurality of instructions for selecting the path from the second set of paths.

24. A design analysis tool capable of interfacing between a static analysis tool and an automatic test pattern generation (ATPG) tool, capable of identifying false paths within a circuit design, and stored via a computer readable medium, said computer readable medium comprising:

a first plurality of instructions for receiving a first set of paths corresponding to the circuit design;

a second plurality of instructions for providing a set of conditions corresponding to at least one path of the first set of paths to the ATPG tool, the ATPG tool having an ATPG model corresponding to at least a portion of the circuit design;

a third plurality of instructions for receiving a response to the set of conditions generated by the ATPG tool using the ATPG model; and

a fourth plurality of instructions for identifying a false path within the first set of paths based on the response from the ATPG tool.

25. The computer readable medium of claim 24, further comprising a fifth plurality of instructions for translating the first set of paths after receiving the first set of paths.

26. The computer readable medium of claim 24, further comprising:

a fifth plurality of instructions for extracting a second set of paths from the first set of paths, wherein the set of conditions corresponds to at least one path of the second set of paths.

27. The computer readable medium of claim 24, wherein the set of conditions comprises at least one of final value conditions, initial value conditions, side propagation value conditions, and slower path conditions.

28. The computer readable medium of claim 27, wherein the response to the set of conditions from the ATPG tool indicates whether the set of conditions is satisfied.

29. The computer readable medium of claim 24, further comprising a fifth plurality of instructions for providing the false path to the static analysis tool.

30. The method of claim 24, wherein the ATPG tool is a commercially available ATPG tool.

31. The method of claim 24, wherein the first set of paths is received from a static analysis tool.